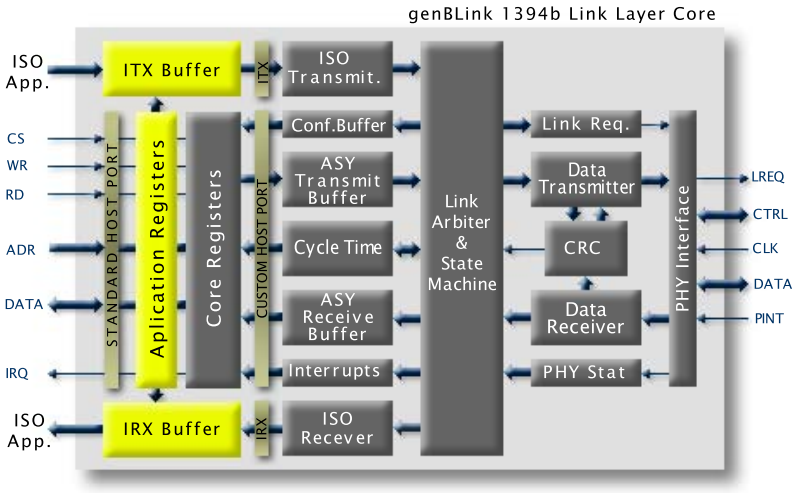


Features

The genBLink™ core is member of ATRA Vision xBLink® family of customized embedded 1394b Link Layer Controllers.

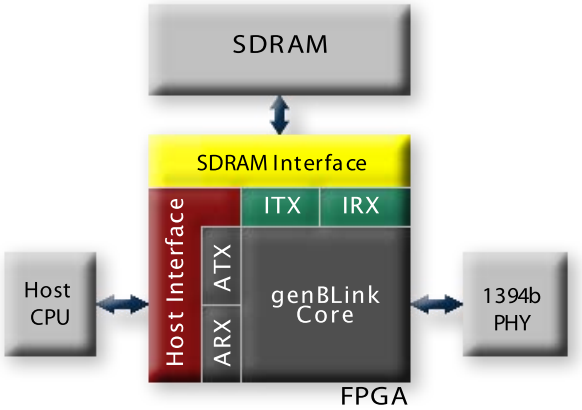
With this core, a designer can build a bilingual 1394a/1394b Node Device with a full Isochronous Transmit, Isochronous Receive and Cycle Master Capabilities.

- Fully compliant with the IEEE standard for High-Performance Serial Bus IEEE Std 1394b™ -2002.
- Supports all standard 1394 Asynchronous, Isochronous and PHY packets.
  - Maximum Isochronous data payload of 8KB.
  - Maximum Asynchronous data payload of 4KB. *
  - S100-S400 Legacy 1394a and S100-S800 Beta 1394b Packet Transmission speed.
- Asynchronous and Isochronous Receive and Transmit Data Buffer implemented with Xilinx® Block Select RAM™ memory.
- Performs CRC packet header and data payload checksum/generation.
- Receives/Transmits Cycle-Start packets.
- 8-bit or 32bit Asynchronous generic Host CPU interface with
  - 32 internal Control, Status and Interrupt Registers.
  - Software polling or Interrupt driven API.
  - Supports data burst accesses and Big/Little Endian Modes.
- Simple ISO Receive/Transmit Data Port interfaces for custom User Application. Supports fixed or variable size data payload.
- Minimum size FPGA footprint for cost and power sensitive embedded applications. Optimized for low cost Xilinx® Spartan3™ FPGA family.
- Hardware tested design with:
  - TSB81BA3 PHY (TI® Physical Interface Chip)
  - XC3S400-PQ208 (Spartan3 TM FPGA).
  - Win 2000/XP® 1394b drivers.

Core Facts	
Device Family	Spartan-3
System Clock	98.304 MHz
Device Features Used	Block Select RAM™, Slice RAM , SHIFT
Link Core Resources	
GCLKs / IOBs	1 / 17
4-input LUTs	953
FFs	653
BRAMS (2KB)	4
Core Registry	
GCLKs / IOBs	1 / 20
4-input LUTs	208
FFs	115
XC3S400 Resources Used	
Link Core	~10%
Core Registry	~5%
ISO Application	~20%
Provided with Core	
Design File Formats	NGC Netlist VHDL Instantiation VHDL Source code
Constraints Files	User Constrain File (UCF)
Verification tools	VHDL Test Bench
Documentation	genBLink Data Sheet
Design Tools Requirements	
Tested Entry / Verification Tools	Xilinx ISE 6.2.03i. MTI ModelSim
Reference Designs	
xBLink Development board.	ISO Transmitter/Receiver Application. Host Transaction Layer Software. Win 2000/XP® Device Driver and Debugging Tools.

Licensing Models	Eval.	Stand.	Custom	Full
Link Core	FPGA bit stream	Xilinx NGC netlist	NGC	VHDL source code
Core Reg.			VHDL	
Appl. Reg.		VHDL source code		
ISO Rec/Tran.		VHDL source code		

Typical Application



Link Layer Services

The genBLink controller supports all standard Asynchronous and Isochronous Link Layer Services

- Link-PHY Protocol,
- Reception and Transmission of 1394 Packets,
- Bus Arbitration,
- Packet Formatting and Decoding,
- CRC generation and Checksum.

The core interfaces directly to 1394b PHY chip and provides three User Interface Ports:

- HOST Port for Asynchronous Transactions and
- ITX Ports for Isochronous Transmit Operations.
- IRX Port for Isochronous Receive Operations.

Asyncronous Transactions

The Asynchronous Transaction Layer Services are carefully split between hardware/software implementation.

Link Layer Core handles real-time constrained services like:

- Transmission and Reception of ACK packets.
- 1394 Packet Data buffering.
- Reception of Cycle Start Packets.

Host CPU controller handles other higher-level transaction services like:

- Interpretation of received Acknowledge packets.

- Transaction Time-outs and Retry Protocol.

ASY Receive and Transmit Data Buffers are implemented with 2KB internal BRAM memories. Received Acknowledge packets are stored in 16-word deep SLICE RAM Confirmation Buffer.

Isochronous Transactions

The core ISO Transmitter/Receiver Modules interfaces to user ISO Application and perform ISO Packet formatting.

The implementation of ISO Data buffers is left outside of genBLink core, leaving System designer with flexibility to make important cost-performance design tradeoffs.

ISO Data Buffers are typically implemented with internal BRAM or external SRAM/SDRAM memory.

Host Interface

Host Controller accesses the Link Layer core through genBLink Register file. Host Port is 8-bit wide generic asynchronous data interface compatible with wide range of CPU controllers.

Development Platform

The genBLink controller comes with flexible Prototype Board and Reference Design KIT.

It is a highly recommended platform for evaluation, integration and development of custom designs based on genBLink core.

Reference Design examples, in full VHDL/C source code, are provided for:

- ISO Transmit/Receive Data Buffers with
  - 16KB internal BRAM memory or
  - external SRAM/SDRAM memories.
- Host ASY Transaction Layer software.

For product documentation / additional information please contact:

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