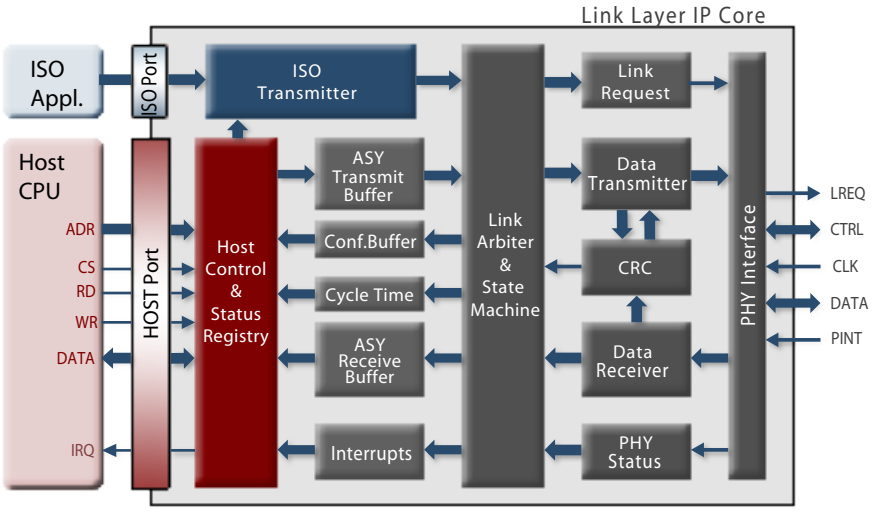
CamBLink™ 1394b Link Layer Controller IP Core



Introduction

The camBLink™ is the first product in the Atra Vision family of a customized embedded 1394b Link Layer Controllers.
With this core, a designer can build bilingual 1394a/1394b Digital Camera, with a maximum packet speed of 800Mbit/s.

Features

- Fully compliant with the IEEE standard for High-Performance Serial Bus - IEEE Std 1394b™-2002.
- Optimized for design requirements of 1394 Trade Association's IIDC Digital Camera Specification, V1.30.

- Hierarchical layered architecture with distinct Link Layer, Transaction Layer and ISO Layer modules.

- Supports all standard 1394 Asynchronous, Isochronous and PHY packets.
- Maximum Isochronous data payload 8KB.
- Maximum Asynchronous data payload 64 Quadlets.
- Support Legacy (1394a) and Beta (1394b) packet with S100, S200, S400 and S800 data transmition speed.

- Asynchronous Receive and Transmit Data Buffer implemented with Xilinx® Block Select RAM™ memory: 1KB ASY Receive Buffer, 1KB ASY Transmit Buffer.

- Inspects and generates CRC packet header and data checksum.
- Receives CycleStart packets and implements internal Cycle Timer.

- 8-bit asynchronous generic Host CPU interface,
- 32 internal Control/Status/Interrupt Registers, and
- Software polling or interrupt driven API.

- Supports Isochronous Transmit Operations with fixed or variable size data payload.
- Simple ISO Transmit Data Port interface to custom Application.

- Minimum size FPGA footprint for cost and power sensitive embedded applications.
- Designed and optimized for low cost Xilinx® Spartan™ FPGA family.

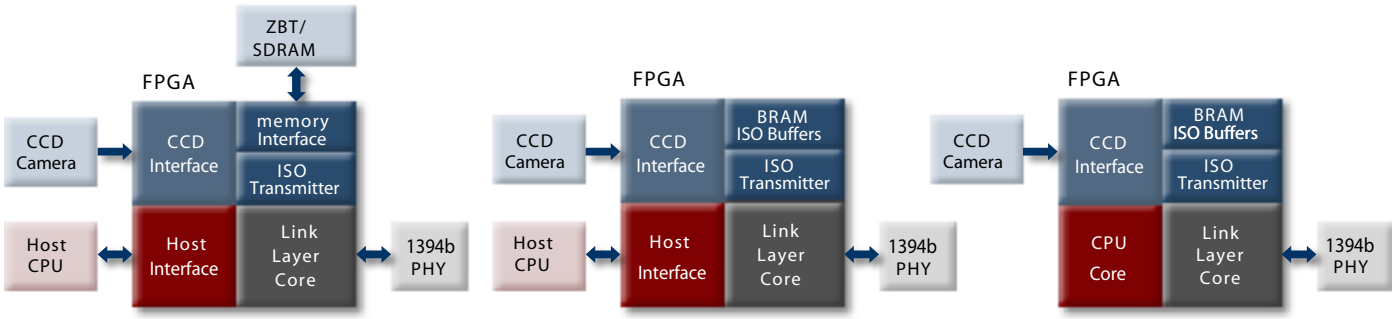
- Fully verified and tested design with:
  - TSB81BA3 PHY (TI® Physical Interface Chip)
  - XC2S200E-PQ208 (Spartan-2E FPGA)

Core Facts		
Device Family	Spartan2E / Spartan3	
System Clock	98.304 MHz	
Device Features Used	Block Select RAM Slice RAM Slice SHIFT Tri-state busses	
Resources Used		
4-input LUTs	764	
FFs	746	
IOBs	16	
GCLKs	2	
Percent CLB Used		
XC2S200E /XC3S200	FFs	LUTs
	~15%	~15%
Provided with Core		
Design File Formats	NGO Netlist VHDL instantiation and simulation Model VHDL Source code	
Constraints Files	User Constrain File (UCF)	
Verification tools	VHDL Test Bench	
Documentation	camBLink Data Sheet camBLink User Manual	
Design Tools Requirements		
Tested Entry / Verification Tools	Xilinx ISE 6.2i. XST or Synplify. MTI ModelSim	
Reference Designs		
xBLink Design KIT with prototype board	ISO Transmitter Application. Host Transaction Layer Software. 1394 Digital camera protocol API. Win2000/XP® Device driver and Debugging Tools.	

Licensing Models

	Evaluation	Standard	Custom	Full
Link Core	FPGA Bit Stream	Xilinx NGO netlist	NGO netlist	VHDL source code
Host Control Registry			VHDL source code	
ISO Transm. Example		VHDL source		

Typical Applications



1394b Camera with external ISO Buffers and discrete CPU

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Fully Integrated Device

Link Layer Services

camBLink controller supports all standard Asynchronous and Isochronous Link Layer Services:

- Link-PHY Protocol,
- Reception and Transmition of 1394 Packets,
- Bus Arbitration,
- Packet Formatting and Decoding,
- CRC generation and Checksum.

The core interface directly to 1394b PHY chip and provides two User Interface Ports:

- HOST Port for Asynchronous Transactions and
- ITX Ports for Isochronous Transmit Operations.

Asynchronous Transactions

To minimize the size of FPGA footprint the Asynchronous Transaction Layer Services are carefully split between hardware/software implementation.

Link Layer Core handles the real-time constrained services like:

- Transmition and Reception of ACK packets.
- 1394 Packet Data buffering.
- Reception of Cycle-Start Packets.

Host CPU controller handles other higher-level transaction services like:

- Interpretation of received Acknowledge packets.
- Transaction Time-outs and Retry protocol.

Receive and Transmit ASY Data Buffers are implemented with 1KB internal BRAM memories.
Received Acknowledge packets are stored in, 16-word deep, Slice Ram Confirmation Buffer.

Isochronous Transactions

The core ISO Transmitter Module interfaces to user ISO Application and perform ISO Packet formatting.

The implementation of ISO Data buffers is left outside of camBLink core.
System designer has flexibility to make important cost-performance design tradeoffs.

ISO Data Buffers are typically implemented with internal BRAM or external SRAM/SDRAM memory.

Host Controller

Host accesses the Link Layer core through Control & Status Register file.
Host Port is 8-bit wide generic asynchronous data interface compatible with wide range of CPU controllers.

Design KIT

The CamBLink controller comes with flexible Prototype Board and Reference Design KIT xBLink.
It is a highly recommended platform for evaluation, integration and development of custom designs based on camBLink core.

Reference Design examples, in full VHDL/C source code, are provided for:

- ISO Transmit Data Buffers with internal BRAM memory.
- ISO Transmit Data Buffers with external ZBT SRAM.
- Host Transaction Layer software driver.
- IIDC 1394-based Digital Camera API

For full product documentation
or additional information please contact

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camBLink Documentation

camblink_fly.pdf	IP Core product Brief
camblink_ds.pdf	IP Core Data Sheet
camblink.pdf	User Manual
xblink_ds.pdf	Development Board Data Sheet